UNDER EMBARGO UNTIL MONDAY, FEBRUARY 4th, 2001

Intel at the IEEE International Solid-State Circuits Conference (ISSCC)

Briefing Packet

Intel Corporation
January 29, 2001

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Introduction

Intel will present eleven papers at the 48th annual IEEE International Solid-State Circuits Conference (ISSCC), taking place in San Francisco from Feb. 3-7. The theme of the conference this year is "ICs for Information Technologies."

The Intel papers will address topics such as circuit design for efficient power management, technologies that will be used in the next-generation Itanium™ microprocessors and promising research findings for advanced Flash memory chips. Intel will also participate in workshops and discussion panels at the conference.

ISSCC: General Information

IEEE International Solid-State Circuits Conference (ISSCC)
February 3-7, 2001
Conference Theme, *ICs for Information Technologies*
San Francisco Marriott Hotel
Web: http://www.isscc.org/

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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Intel Technical Papers at ISSCC: Abstracts and Presentation Schedule

Circuit Design Papers

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1. Invited Paper (Part of ISSCC Special Topic Evening Sessions): *Low-Voltage Design for Portable Systems: Leakage Reduction in Digital CMOS Circuits*

Sunday, Feb. 3, 7:30 p.m.
Presenter: Shekhar Borkar, Intel Fellow

2. Technical Paper: *1.1V 1GHz Communications Router with On-Chip Body Bias in 150nm CMOS*

Session 16: High-Speed Circuit Techniques and I/O
Tuesday, Feb. 5, 3:15 p.m.
A router chip, that incorporates on-chip forward body biasing capability with 2% area overhead, achieves 1GHz operation at 1.1V supply in a 150nm logic technology, compared to 1.25V required for the original design having no body bias. Switching power is 23% less and chip leakage is reduced by 3.5x in standby mode by withdrawing forward bias.

3. Technical Paper: *A 6.5GHz 130nm Single-Ended Dynamic ALU and Instruction-Scheduler Loop*

Session 25: Processor Building Blocks
Wednesday, Feb. 6, 1:30 p.m.
32b Han-Carlson ALU and 8-entry x 2-ALU-instruction scheduler loop for 6.5GHz single-cycle integer execution at 1.2V and 25°C use dual-Vt CMOS technology. A single-ended, leakage-tolerant dynamic scheme enables up to 9-wide ORs with 23% critical path speed improvement, 40% active leakage power reduction compared to Koggie-Stone implementation, dense layout occupying 44,100? m^2, and performance scaleable to 8GHz at 1.5V, 25°C.

4. Technical Paper: *5GHz 32b Integer-Execution Core in 130nm Dual-V_t CMOS*

Session 25: Processor Building Blocks
Wednesday, Feb. 6, 2:00 p.m.
A 32b integer execution core implements 12 instructions. Circuit and body bias techniques together increase the core clock frequency to 5GHz. In a 130nm six-metal dual-V_t CMOS process, the 2.3mm^2 prototype contains 160k transistors, with RF-ALU units dissipating 515mW at 1.6V.

5. Technical Paper: ***Adaptive Body-Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage***

Session 25: Processor Building Blocks
Wednesday, Feb. 6, 4:45 p.m.
Measurements on a 150nm CMOS test chip show that on-chip bi-directional adaptive body biasing compensates effectively for die-to-die parameter variation to meet both frequency and leakage requirements. An enhancement of this technique to correct for within-die variations triples the accepted die count in the highest frequency bin.

Intel® Itanium™ Processor Family Papers (these papers will be co-presented with Hewlett Packard)

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1. Technical Paper: ***The 16kB Single-Cycle-Read-Access Cache on a Next-Generation 64b Itanium Microprocessor***

Session 6: Non-Volatile Memories and SRAM
Monday, Feb. 4, 4:15 p.m.
A 16kB four-ported physically addressed cache operates at 1.2GHz with 19.2GB/s peak bandwidth. Circuit and microarchitectural techniques are optimized to allow a single-cycle read access latency. The cache occupies 3.2x1.8mm^2 in a 0.18? m process.

2. Technical Paper: ***An On-Chip 3MB Subarray-Based 3rd-Level Cache for a Next-Generation 64b Itanium Microprocessor***

Session 4: High-Speed Digital Interfaces
Monday, Feb. 4, 4:45 p.m.
This 3MB on-chip level-three cache employs subarray design style, and achieves 85% array efficiency. Characterized to operate up to 1.2GHz, the cache allows a store and a load in every four core cycles, and provides a total bandwidth of 64GB/s at 1.0GHz.

3. Technical Paper: ***The Core Clock System for a Next-Generation Itanium Processor***

Session 8: High-Speed Timing
Tuesday, Feb. 5, 10:45 a.m.
A PLL generates a high-frequency core clock for a 1GHz processor by multiplying up the system clock. The clock is distributed across the 19x14mm core via a shielded, balanced, H-tree to the

final pulsed gated buffers with <62ps measured skew. Test features include phase shrinking and regional skew manipulation.

4. Technical Paper: ***The Implementation of the Next-Generation 64b Itanium Microprocessor***

Session 20: Microprocessors
Wednesday, Feb. 6, 11:15 a.m.
The processor incorporates over 220M transistors on a 464mm^2 die and operates at >1.2GHz with an 8-stage pipeline in a 0.18? m process. It has three levels of on-chip cache totaling over 3.3MB providing >32GB/s bandwidth at each level.

5. Technical Paper: ***The High-Bandwidth 256kB 2nd-Level Cache on an Itanium Microprocessor***

Session 25: Processor Building Blocks
Wednesday, Feb. 6, 3:45 p.m.
A second-level 256kB unified cache is incorporated into a 1.2GHz next-generation Itanium microprocessor. The datapath structures provide a non-blocking, out-of-order interface to the processor core achieving a minimum 5-cycle latency with a stand-alone bandwidth of 72GB/s.

6. Technical Paper: ***The Fully-Bypassed 6-Issue Integer-Integer Datapath and Register File on an Itanium Microprocessor***

Session 25: Processor Building Blocks
Wednesday, Feb. 6, 4:15 p.m.
A 6-issue integer datapath with a 20 ported 128x65b register file in a 0.18? m process operates up to 1.2GHz at 1.5V. Operands bypass through 4 stages, from 34 locations, using ½ clock for execution and ½ clock for bypass. Each result is available for the next instruction.

Next-Generation, Non-Volatile Memory Paper

Contact: Dan Francisco, (916) 356-0546, daniel.j.francisco@intel.com

1. Technical Paper: ***Ovonic Unified Memory – A High-Performance Non-volatile Memory Technology for Stand-Alone Memory and Embedded Applications***

Session 12: Digital Directions
Tuesday, Feb. 5, 3:15 p.m.
Development status of Ovonic unified memory (OUM), a phase-change non-volatile semiconductor memory technology is discussed. Using 0.18? m 3V CMOS, cells from 5F^2 to 8F^2

are built in a charge-pump-free 4Mb development vehicle. Direct overwrite, 10ns reset times, 50ns set times, and $1.0x10^{12}$ cycling are achieved. Ten-year data retention is projected at $120^{o}C$.

Other Intel Activities at ISSCC

1. Discussion Session: *When Will Optical Interconnects Appear on High-Performance Microprocessors*

Monday, Feb. 4, 8:00 p.m.
Moderator: Ian Young, Intel Fellow
Performance of modern processors is limited not by intrinsic transistor speed, but by bandwidth and latency of internal and external interconnects. Optical interconnect technology promises virtually unlimited bandwidth. Will large-scale digital chips be forced to use optical interconnects on-chip and to the rest of the system? Will on-chip copper interconnects with mixed signal I/O and DSP techniques enable microprocessors to remain purely electrical chips? Are the cost/performance advantages of opto-electronics attractive enough to overcome the inertia of a mature industry?

2. Discussion Session: *Low-Voltage Design or the End of MOSFET Scaling?*

Tuesday, Feb. 5, 8:00 p.m.
Panelist: Shekhar Borkar, Intel Fellow
CMOS feature size continues to shrink for digital circuits, and mass production in 0.1? m is in sight. Yet, the trend of decreasing supply voltage in deep sub-micron processes tends to make analog and memory circuit design harder. The panel focuses on two issues: (1) How low-voltage can CMOS circuit designs be? (2) Without scaling, is it possible to continue improving performance and reducing cost of CMOS LSI?

3. Workshop on Microprocessor Design

Thursday, Feb. 7, 8:30 a.m. – 5:15 p.m.
This workshop includes presentations by two Intel speakers, giving presentations on Clocking Impacts on Architecture – future directions, and Architecture implications for Clocking in 10-20GHz processors.